BUILT-IN SELF TEST CIRCUIT USING LINEAR FEEDBACK SHIFT REGISTER

ABSTRACT OF THE DISCLOSURE

A built-in self test (BIST) circuit comprising a linear feedback shift register is disclosed. The BIST circuit comprises a controller for controlling a self-testing operation of a memory chip embedded in an integrated circuit, an address generator for generating pseudo-random address patterns under control of the controller, a data generator for producing test data associated with data backgrounds of the address bits under the control of the controller, and a comparator for comparing the test data with memory data output from the memory chip to detect a defect, if any, of the memory chip. The pseudo-random random pattern comprises a single-random pseudo-random address pattern.